What is claimed is:

1. A layout method of a comparator array of a flash type analog to digital converting circuit, the flash type analog to digital converting circuit including: (i) a reference voltage for generating 2^n voltages and being arranged to be folded; (ii) a comparator array including (2^n-1) comparators for comparing voltage differences between the respective 2^n voltages and an analog input signal to generate a digital signal having (2^n-1) thermometer codes; and (iii) an encoder for encoding the digital signal having (2^n-1) thermometer codes to generate an n-bit of digital signal,

the layout method comprising:

arranging the comparators such that the comparators of $(2^n-1)^{th}$ comparator to $(2^n/2)^{th}$ comparator are arranged in order and the comparators of $(2^n/2\text{-}1)^{th}$ comparator to a first comparator are arranged in a reverse fashion between the comparators of the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator; and

arranging the comparators such that the neighboring comparators adjacent to the respective (2^n-1) comparators transit to the same state when the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator transit to different states respectively.

2. The layout method of claim 1, wherein each of the (2^n-1) comparators includes a positive input and output terminal and a negative input and output terminal, and the comparators of the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator are arranged in order of the positive input and output terminal, the negative input and output terminal, the positive input and output terminal, the negative input and output terminal, the negative input and output terminal, the positive input and

output terminal, the negative input and output terminal, and the positive input and output terminal.

3. The layout method of claim 1, wherein each of the (2^n-1) comparators includes a positive input and output terminal and a negative input and output terminal, and the comparators of the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator are arranged in order of the negative input and output terminal, the positive input and output terminal, the negative input and output terminal, the positive input and output terminal, the positive input and output terminal, the negative input and output terminal, the positive input and output terminal, and the negative input and output terminal.

4. The layout method of claim 1, wherein the comparator array includes first and second dummy comparators, the first dummy comparator arranged adjacent to the $(2^n-1)^{th}$ comparator, the second dummy comparator arranged adjacent to $(2^n/2)^{th}$ comparator,

wherein the comparators of the first dummy comparator to the second dummy comparators includes positive and negative input and output terminals, respectively, and the comparators of the first dummy comparator to the second dummy comparators are arranged in order of the positive input and output terminal, the negative input and output terminal, the positive input and output terminal, the negative input and output terminal, the negative input and output terminal, the

positive input and output terminal, the negative input and output terminal, and the positive input and output terminal.

5. The layout method of claim 4, wherein the second dummy comparator is configured such that a reference voltage and an analog input signal applied to the positive input terminal of the $(2^n/2\text{-}1)^{th}$ comparator are applied to the positive input terminal of the second dummy comparator, and a reference voltage and an analog input signal applied to the negative input terminal of the $(2^n/2\text{-}1)^{th}$ comparator are applied to the positive input terminal of the second dummy comparator.

6. The layout method of claim 1, wherein the the comparator array includes first and second dummy comparators, the first dummy comparator arranged adjacent to the $(2^n-1)^{th}$ comparator, the second dummy comparator arranged adjacent to $(2^n/2)^{th}$ comparator,

wherein the comparators of the first dummy comparator to the second dummy comparators includes positive and negative input and output terminals, respectively, and the comparators of the first dummy comparator to the second dummy comparators are arranged in order of the negative input and output terminal, the positive input and output terminal, the negative input and output terminal, the positive input and output terminal, the positive input and output terminal, the negative input and output terminal, the positive input and output terminal, and the negative input and output terminal.

7. The layout method of claim 6, wherein the second dummy comparator is configured such that a reference voltage and an analog input signal applied to the positive input terminal of the $(2^n/2\text{-}1)^{th}$ comparator are applied to the positive input terminal of the second dummy comparator, and a reference voltage and an analog input signal applied to the negative input terminal of the $(2^n/2\text{-}1)^{th}$ comparator are applied to the positive input terminal of the second dummy comparator.

8. A layout method of a comparator array, comprising:

among (2^n-1) comparators for comparing voltage differences between each of 2^n voltages and an analog input signal to generate a digital signal having (2^n-1) thermometer codes,

arranging the comparators such that the comparators of $(2^n-1)^{th}$ comparator to $(2^n/2)^{th}$ comparator are arranged in order and the comparators of $(2^n/2\text{-}1)_{th}$ comparator to a first comparator are arranged in reverse fashion between the comparators of the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator; and

arranging the comparators such that the neighboring comparators adjacent to the respective (2^n-1) comparators transit to the same state when the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator transit to different states respectively.

9. The layout method of claim 8, wherein each of the (2^n-1) comparators includes a positive input and output terminal and a negative input and output terminal, and the comparators of the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator are arranged in order of the positive input and output terminal, the negative input and output terminal, the positive input and output terminal, the negative input and

output terminal, the negative input and output terminal, the positive input and output terminal, the negative input and output terminal, and the positive input and output terminal.

10. The layout method of claim 8, wherein each of the (2^n-1) comparators includes a positive input and output terminal and a negative input and output terminal, and the comparators of the $(2^n-1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator are arranged in order of the negative input and output terminal, the positive input and output terminal, the negative input and output terminal, the positive input and output terminal, the positive input and output terminal, the negative input and output terminal, the positive input and output terminal, and the negative input and output terminal.